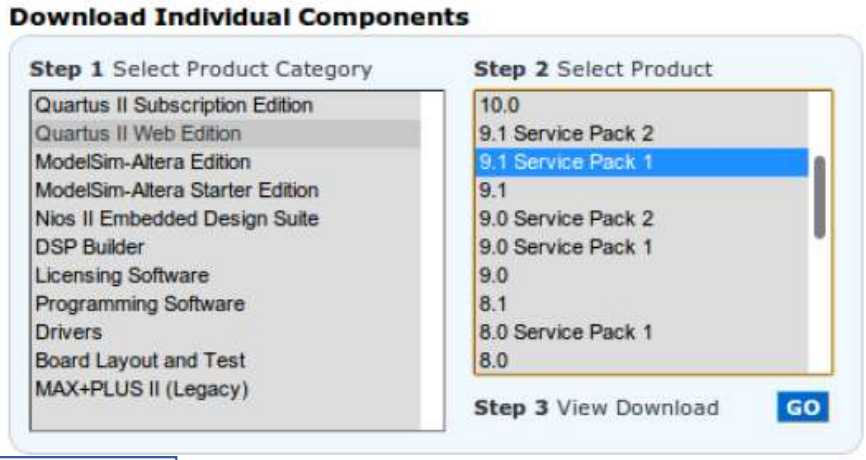
Quartus II Web Edition v9.1 Service Pack 1

1) Go to : https://www.altera.com/download/dnl-index.jsp
2) Scroll down to download individual components and select Quartus II Web Edition in 'Step 1'
3) In 'Step 2' scroll down and select '9.1 Service Pack 1' and press OK



Quartus II

Web Edition

Free

9.1

ModelSim

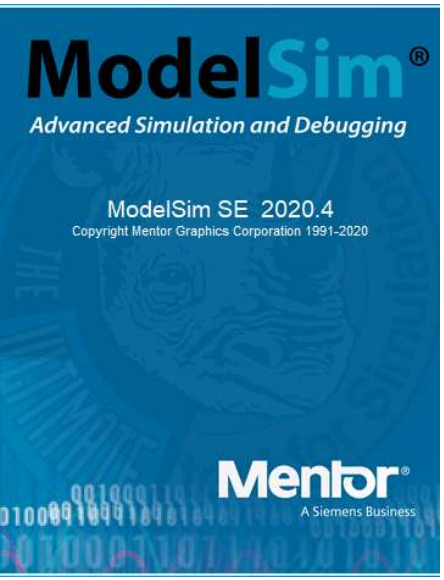
On ne: ır Windows or Linux Operating Systems

date: Ja

II Web

load Op

Quartus II Web Edition	Platform	File Name	Size
Quartus II Web Edition Service Pack 1	Windows	91sp1_quartus_free.exe	1.5 GB
Quartus II Web Edition Service Pack 1	Linux	91sp1_quartus_free_linux.tar	1.8 GB



ModelSim SE-64 2020.4

File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help

Help

Layout NoDesign ColumnLayout AllColumns

Library

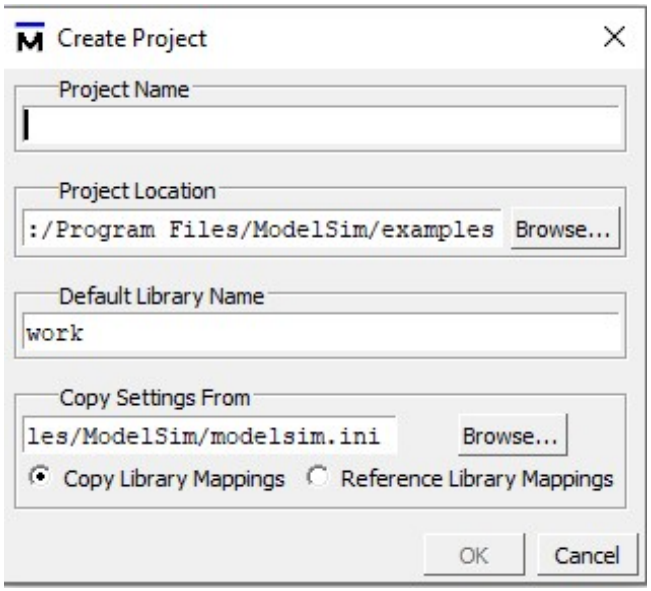
Name	Type	Path
floatfixlib	Library	$MODEL_TECH/../floatfixlib
flps_lib	Library	$MODEL_TECH/../flps_lib
ieee_env (empty)	Library	$MODEL_TECH/../ieee_env
infact	Library	$MODEL_TECH/../infact
mc2_lib	Library	$MODEL_TECH/../mc2_lib
mgc_ams (empty)	Library	$MODEL_TECH/../mgc_ams
mtiAvm	Library	$MODEL_TECH/../avm
mtiOvm	Library	$MODEL_TECH/../ovm-2.1.2
mtiPA (empty)	Library	$MODEL_TECH/../pa_lib
mtiRnm	Library	$MODEL_TECH/../rnm
mtiUPF	Library	$MODEL_TECH/../upf_lib
mtiUvm	Library	$MODEL_TECH/../uvm-1.1d
osvvm	Library	$MODEL_TECH/../osvvm
sv_std	Library	$MODEL_TECH/../sv_std
vh_ux01v_lib	Library	$MODEL_TECH/../vh_ux01v_lib
vhdlopt_lib	Library	$MODEL_TECH/../vhdlopt_lib
vital2000	Library	$MODEL_TECH/../vital2000
ieee	Library	$MODEL_TECH/../ieee
modelsim_lib	Library	$MODEL_TECH/../modelsim_lib
std	Library	$MODEL_TECH/../std
std_developerskit	Library	$MODEL_TECH/../std_developerskit
synopsys	Library	$MODEL_TECH/../synopsys
verilog	Library	$MODEL_TECH/../verilog

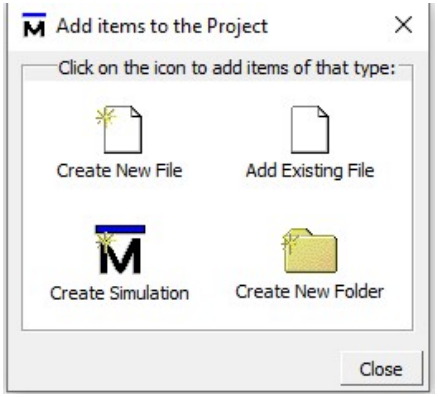
Transcript

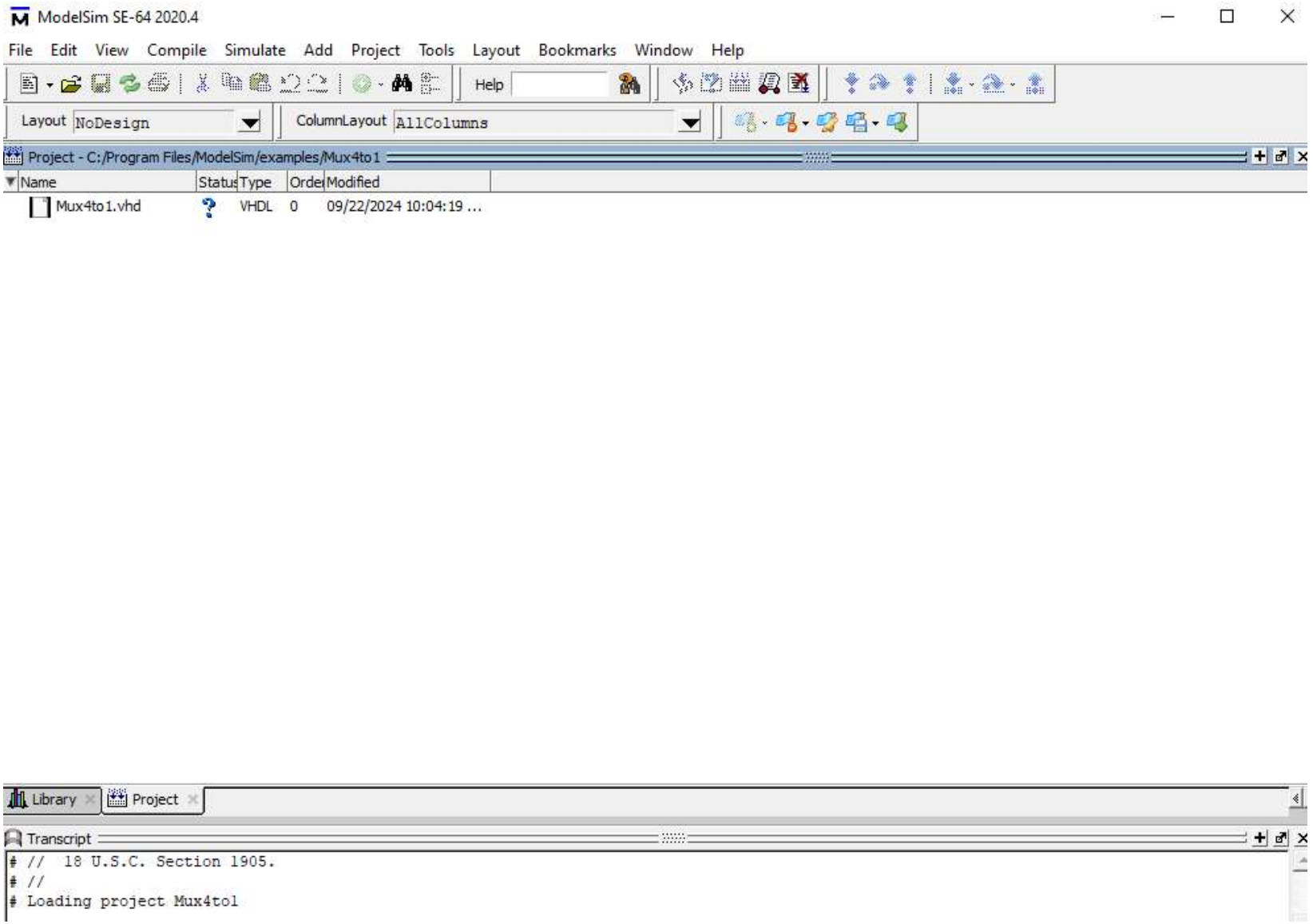
```
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
```

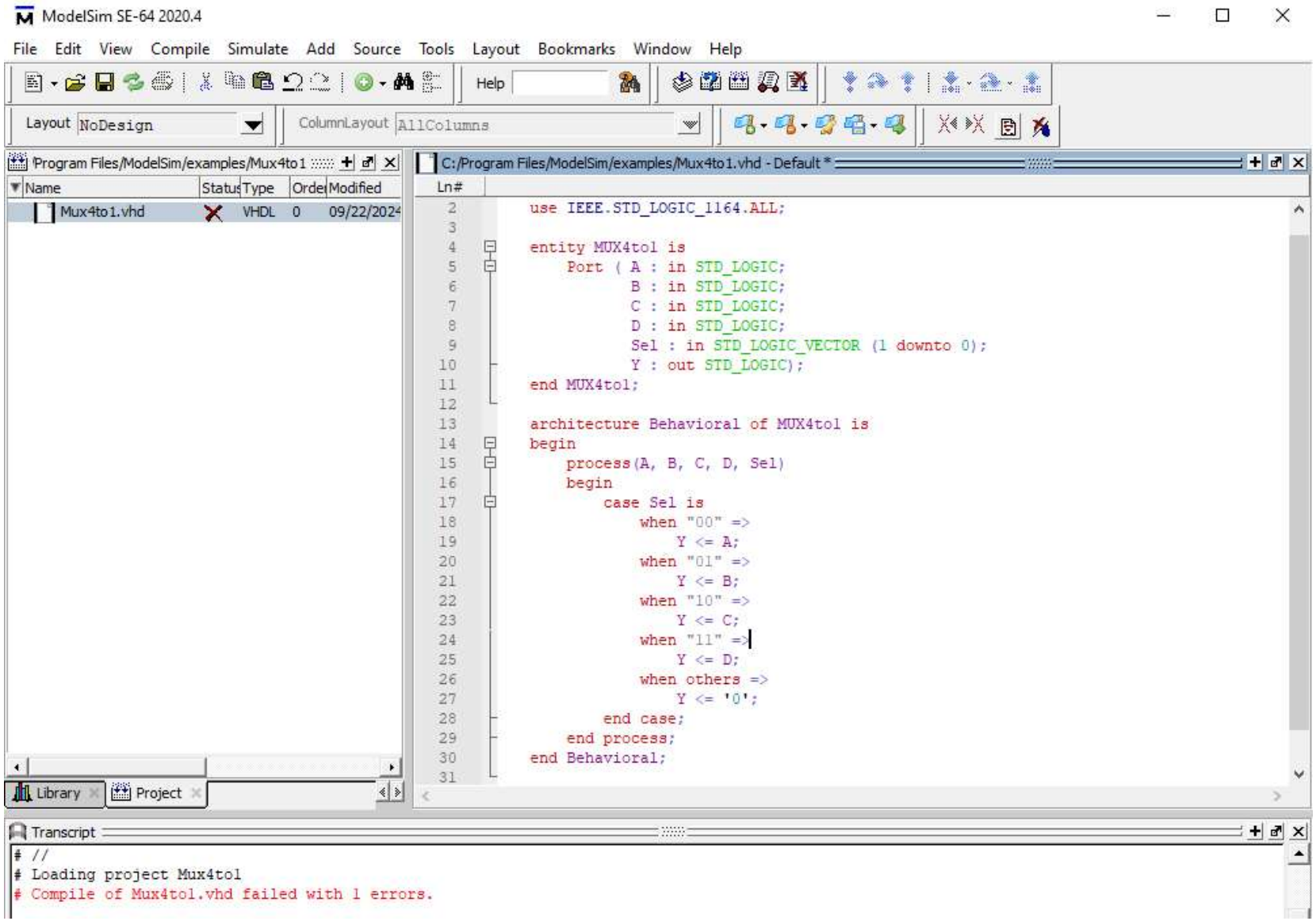
ایجاد پروژه در Model Sim

- After installation → read me. Tex
- File → new → project

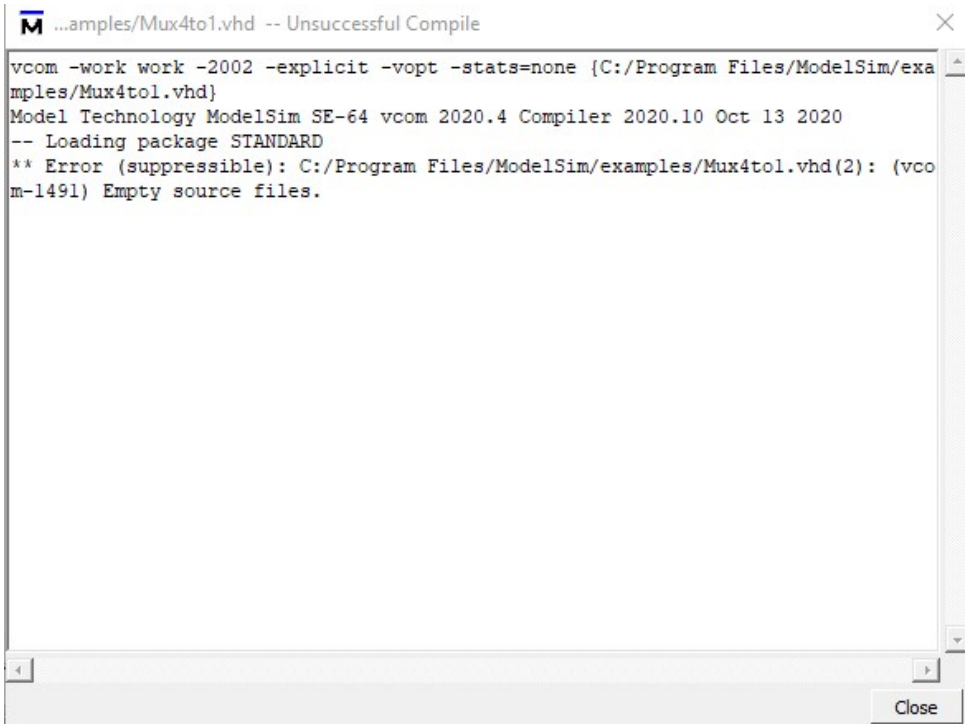


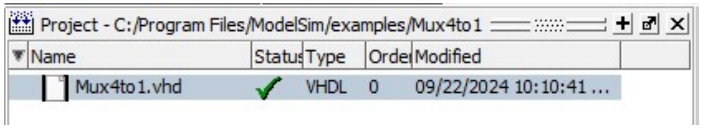



ModelSim SE-64 2020.4
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Project - C:/Program Files/ModelSim/examples/Mux4to1
Name Status Type Order Modified
Mux4to1.vhd VHDL 0 09/22/2024 10:04:19 ...
Library
Project
Transcript
// 18 U.S.C. Section 1905.
//
Loading project Mux4to1


ModelSim SE-64 2020.4
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Program Files/ModelSim/examples/Mux4to1
Name Status Type Order Modified
Mux4to1.vhd VHDL 0 09/22/2024
Library
Project
C:/Program Files/ModelSim/examples/Mux4to1.vhd - Default *
Ln#
2 use IEEE.STD_LOGIC_1164.ALL;
3
4 entity MUX4to1 is
5 Port (A : in STD_LOGIC;
6 B : in STD_LOGIC;
7 C : in STD_LOGIC;
8 D : in STD_LOGIC;
9 Sel : in STD_LOGIC_VECTOR (1 downto 0);
10 Y : out STD_LOGIC);
11 end MUX4to1;
12
13 architecture Behavioral of MUX4to1 is
14 begin
15 process(A, B, C, D, Sel)
16 begin
17 case Sel is
18 when "00" =>
19 Y <= A;
20 when "01" =>
21 Y <= B;
22 when "10" =>
23 Y <= C;
24 when "11" =>
25 Y <= D;
26 when others =>
27 Y <= '0';
28 end case;
29 end process;
30 end Behavioral;
31
Transcript
//
Loading project Mux4to1
Compile of Mux4to1.vhd failed with 1 errors.

Save fill and Compile



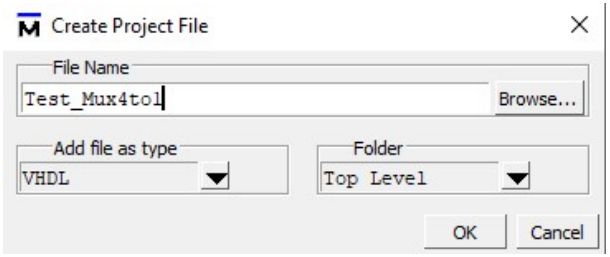


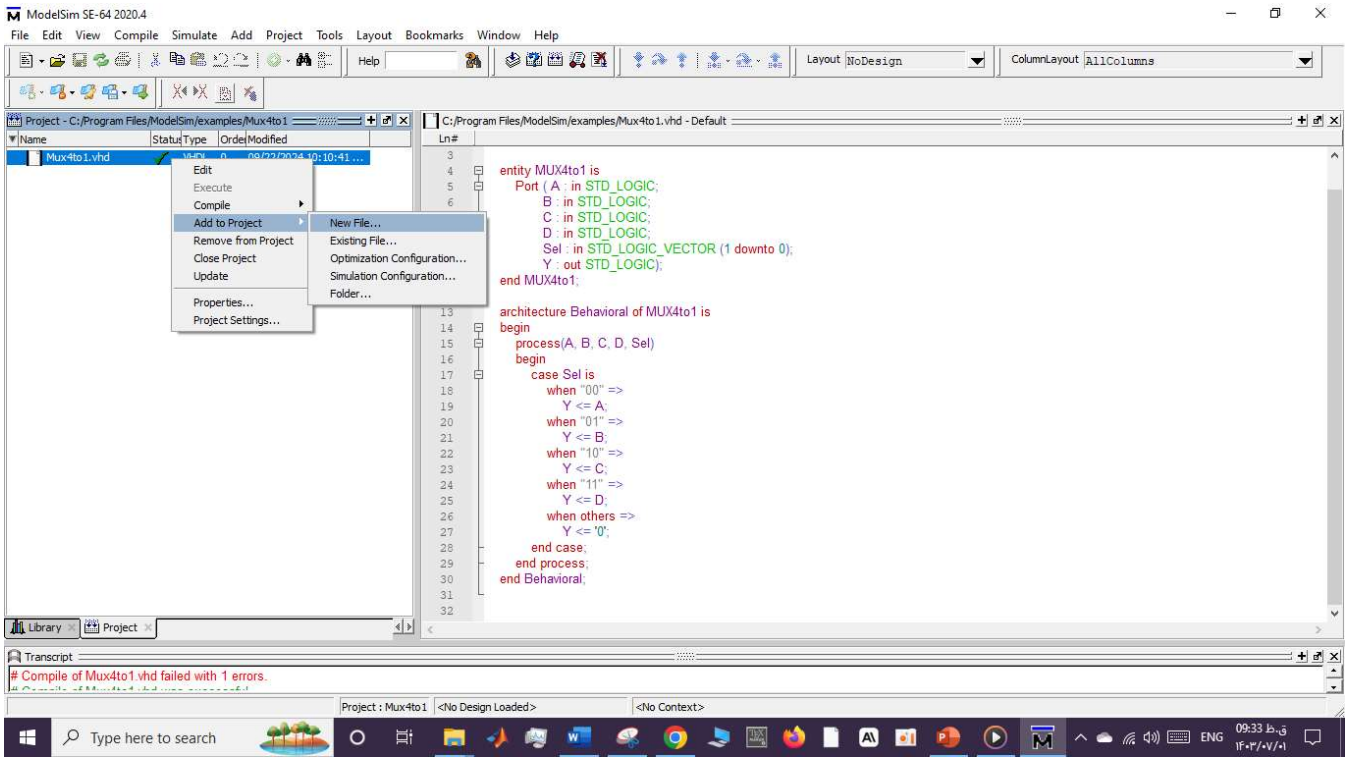
تست بنچ (Testbench) در ModelSim چیست؟

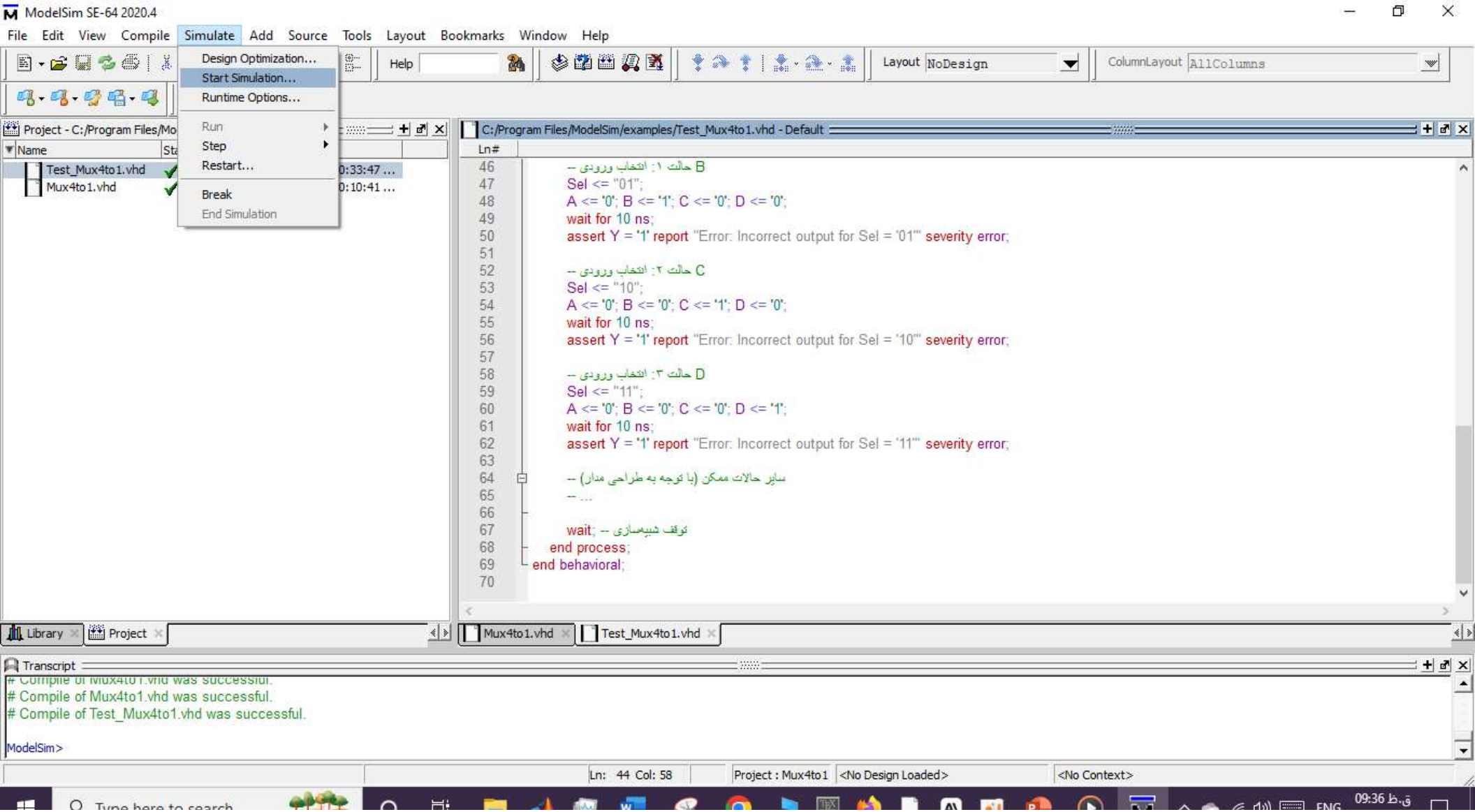
- در محیط شبیه‌سازی مانند ModelSim، تست بنچ یک ماژول یا قطعه کدی است که برای بررسی عملکرد صحیح یک مدار طراحی شده است. به عبارت دیگر، تست بنچ ورودی‌های مختلفی را به مدار اعمال می‌کند و خروجی‌های حاصل را با نتایج مورد انتظار مقایسه می‌کند تا از صحت عملکرد مدار اطمینان حاصل شود.
- **چرا به تست بنچ نیاز داریم؟**
- **تایید صحت طراحی:** قبل از پیاده‌سازی مدار روی سخت‌افزار، با استفاده از تست بنچ می‌توانیم از صحت عملکرد آن اطمینان حاصل کنیم.
- **ایجاد پوشش تست بالا:** با طراحی تست بنچ‌های مناسب، می‌توانیم تمامی حالات ممکن یک مدار را تست کرده و از پوشش تست بالایی اطمینان حاصل کنیم.
- **عیب‌یابی سریع‌تر:** در صورت بروز خطا در مدار، تست بنچ می‌تواند به ما کمک کند تا محل دقیق خطا را شناسایی کنیم.

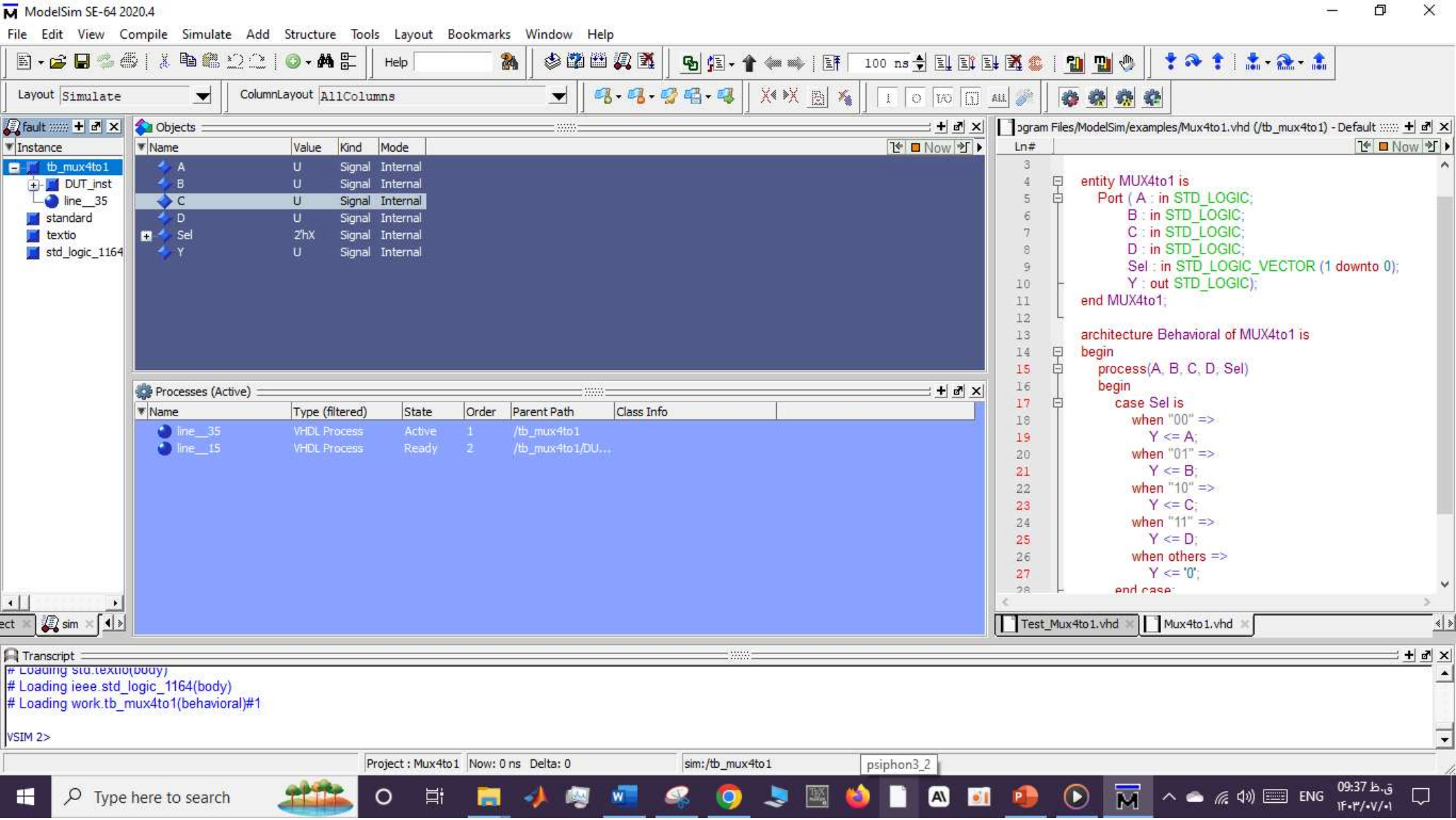
ساختار تست بنچ:

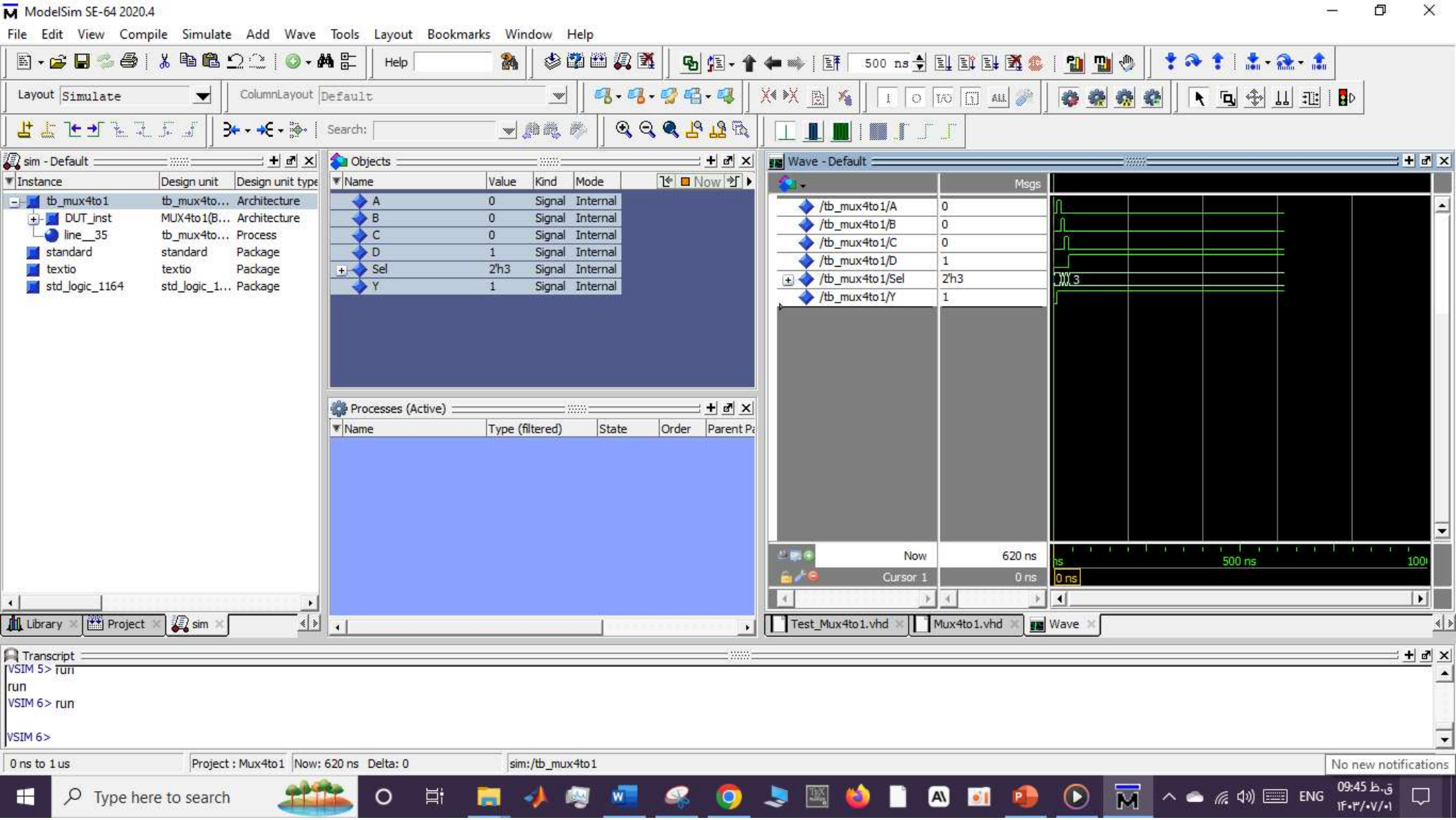
- یک تست بنچ برای این مدار شامل موارد زیر خواهد بود:
- **تعریف ورودی‌ها:** تعریف سیگنال‌های A، B، C، Dو Selبه عنوان ورودی‌های تست بنچ.
- **تعریف خروجی‌ها:** تعریف سیگنال Yبه عنوان خروجی تست بنچ.
- **ایجاد محرک‌ها:** ایجاد یک فرایند یا مجموعه دستوراتی برای اعمال مقادیر مختلف به ورودی‌ها در زمان‌های مختلف.
- **بررسی خروجی‌ها:** مقایسه خروجی‌های حاصل از شبیه‌سازی با مقادیر مورد انتظار.


Create Project File
File Name
Test_Mux4to1
Browse...
Add file as type
VHDL
Folder
Top Level
OK
Cancel


ModelSim SE-64 2020.4
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Project - C:/Program Files/ModelSim/examples/Mux4to1
Mux4to1.vhd
Edit
Execute
Compile
Add to Project
Remove from Project
Close Project
Update
Properties...
Project Settings...
New File...
Existing File...
Optimization Configuration...
Simulation Configuration...
Folder...
C:/Program Files/ModelSim/examples/Mux4to1.vhd - Default
entity MUX4to1 is
Port (A : in STD_LOGIC;
B : in STD_LOGIC;
C : in STD_LOGIC;
D : in STD_LOGIC;
Sel : in STD_LOGIC_VECTOR (1 downto 0);
Y : out STD_LOGIC);
end MUX4to1;
architecture Behavioral of MUX4to1 is
begin
process(A, B, C, D, Sel)
begin
case Sel is
when "00" =>
Y <= A;
when "01" =>
Y <= B;
when "10" =>
Y <= C;
when "11" =>
Y <= D;
when others =>
Y <= '0';
end case;
end process;
end Behavioral;
Transcript
Compile of Mux4to1.vhd failed with 1 errors.
Project : Mux4to1
<No Design Loaded>
<No Context>
Type here to search


ModelSim SE-64 2020.4
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Design Optimization...
Start Simulation...
Runtime Options...
Run
Step
Restart...
Break
End Simulation
Help
Layout NoDesign
ColumnLayout AllColumns
Project - C:/Program Files/Mo
Name
Test_Mux4to1.vhd
Mux4to1.vhd
C:/Program Files/ModelSim/examples/Test_Mux4to1.vhd - Default
Ln#
46 -- حالت ۱: انتخاب ورودی B
47 Sel <= "01";
48 A <= '0'; B <= '1'; C <= '0'; D <= '0';
49 wait for 10 ns;
50 assert Y = '1' report "Error: Incorrect output for Sel = '01'" severity error;
51
52 -- حالت ۲: انتخاب ورودی C
53 Sel <= "10";
54 A <= '0'; B <= '0'; C <= '1'; D <= '0';
55 wait for 10 ns;
56 assert Y = '1' report "Error: Incorrect output for Sel = '10'" severity error;
57
58 -- حالت ۳: انتخاب ورودی D
59 Sel <= "11";
60 A <= '0'; B <= '0'; C <= '0'; D <= '1';
61 wait for 10 ns;
62 assert Y = '1' report "Error: Incorrect output for Sel = '11'" severity error;
63
64 -- سایر حالات ممکن (با توجه به طراحی مدار)
65 -- ...
66
67 wait; -- توقف شبیه‌سازی
68 end process;
69 end behavioral;
70
Library
Project
Mux4to1.vhd
Test_Mux4to1.vhd
Transcript
Compile of Mux4to1.vhd was successful.
Compile of Mux4to1.vhd was successful.
Compile of Test_Mux4to1.vhd was successful.
ModelSim>
Ln: 44 Col: 58
Project : Mux4to1
<No Design Loaded>
<No Context>


ModelSim SE-64 2020.4
File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help
Objects
Name Value Kind Mode
A U Signal Internal
B U Signal Internal
C U Signal Internal
D U Signal Internal
Sel 2'hX Signal Internal
Y U Signal Internal
Processes (Active)
Name Type (filtered) State Order Parent Path Class Info
line__35 VHDL Process Active 1 /tb_mux4to1
line__15 VHDL Process Ready 2 /tb_mux4to1/DU...
entity MUX4to1 is
Port (A : in STD_LOGIC;
B : in STD_LOGIC;
C : in STD_LOGIC;
D : in STD_LOGIC;
Sel : in STD_LOGIC_VECTOR (1 downto 0);
Y : out STD_LOGIC);
end MUX4to1;
architecture Behavioral of MUX4to1 is
begin
process(A, B, C, D, Sel)
begin
case Sel is
when "00" =>
Y <= A;
when "01" =>
Y <= B;
when "10" =>
Y <= C;
when "11" =>
Y <= D;
when others =>
Y <= '0';
Transcript
Loading ieee.std_logic_1164(body)
Loading work.tb_mux4to1(behavioral)#1
VSIM 2>
Project : Mux4to1
Now: 0 ns Delta: 0
sim:/tb_mux4to1
psiphon3_2
Type here to search
ENG


ModelSim SE-64 2020.4
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance Design unit Design unit type
tb_mux4to1 tb_mux4to... Architecture
DUT_inst MUX4to1(B... Architecture
line__35 tb_mux4to... Process
standard standard Package
textio textio Package
std_logic_1164 std_logic_1... Package
Objects
Name Value Kind Mode
A 0 Signal Internal
B 0 Signal Internal
C 0 Signal Internal
D 1 Signal Internal
Sel 2'h3 Signal Internal
Y 1 Signal Internal
Processes (Active)
Name Type (filtered) State Order
Wave - Default
Msgs
/tb_mux4to1/A 0
/tb_mux4to1/B 0
/tb_mux4to1/C 0
/tb_mux4to1/D 1
/tb_mux4to1/Sel 2'h3
/tb_mux4to1/Y 1
Now 620 ns
Cursor 1 0 ns
500 ns
Transcript
VSIM 5> run
run
VSIM 6> run
VSIM 6>
0 ns to 1 us
Project : Mux4to1
Now: 620 ns Delta: 0
sim:/tb_mux4to1
No new notifications
Type here to search
ENG

سایت های مرتبط

1. **Xilinx Vivado Design Suite**:
   https://www.xilinx.com/support/download.html
2. **Intel Quartus Prime**:
   https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/download.html
3. **ModelSim (Mentor Graphics)**:
   https://eda.sw.siemens.com/en-US/ic/modelsim/
4. **ISE Design Suite**:
   https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools/archive-ise.html
5. **Cadence Incisive**:
   https://www.cadence.com/en_US/home/tools.html
6. **Synopsys Design Compiler**:
   https://www.synopsys.com/support.html